CS/ECE 354 Final Examination
Lectures 2 & 3
December 16, 1993

Name: ANSWER Signature:_____

Student ID: _____

Instructor: _____

1. This exam is open book, open notes. NO calculators.
2. Write all answers on the exam.
3. Write your name and student ID on all pages of the exam.

This test consists of 15 questions. Points awarded vary by question.

You have precisely two hours to complete this exam.

Page	Maximum	Score
2	10	
3	13	
4	18	
5	10	
6	19	
Total	70	

1. (4 points) Consider the following MAL code:

```
        .text
         .
         .
         .
        sub   $sp, $sp, 12
        sw    $s3, 12($sp)
        sw    $s4, 8($sp)
        jal   X
        lw    $s3, 12($sp)
        lw    $s4, 8($sp)
        add   $sp, $sp, 12
         .
         .
         .
   X:   sw    $ra, 4($sp)
        lw    $t0, 8($sp)
        lw    $t1, 12($sp)
        bge   $t1, $t0, L1
        sw    $t0, 12($sp)
        sw    $t1, 8($sp)
   L1:  lw    $ra, 4($sp)
        jr    $ra
```

What does procedure X do? Give a description of its function independent of the code that calls it.

Procedure X sorts two parameters passed on the stack.

2. (3 points) Name three types of information that may be stored in a stack frame.

1. parameters
2. registers
3. temporary variables or return address.

3. (3 points) The MIPS R2000 must do the following 3 things atomically to return from exception handling:

1. Restore previous kernel/user mode
2. Enable interrupts
3. Jump back to the previously running code using the EPC

Give a brief example of what might go wrong if these were not accomplished all in one step.

An interrupt might occur before the program returned, leaving the address of the jump instruction in the EPC.

4. (5 points)

```
          .data
Inst:     .word 0x3405abcd
          .word 0x0000000c
          .text
__start:  li    $5, 2
          li    $2, 10
          la    $8, Inst
          jr    $8
          li    $5, 6
          syscall
```

Assume this MAL program is executed without exceptions other than `syscall`. What value will be in register $5 when the exception handler is first invoked?

0x3405abcd disassembles to:
ori $5, $0, 0xabcd
0x0000000c disassembles to:
syscall
Therefore, register $5 = 0xabcf

5. (5 points) The MIPS RISC hardware actually performs delayed branching, executing a single succeeding instruction whether or not the branch is taken. This mode is captured in the simulator by running in *bare mode*. Consider the following code, assuming a delayed-branch model of the MIPS RISC architecture:

```
          li    $s1, 10
loop:     addi  $s1, $s1, -1
          bgtz  $s1, $0, loop
          addi  $s1, $s1, -3
next:     sw    $s1, count
```

How many times will the loop be executed before the instruction labelled `next` is reached? Give the sequence of values assigned to the register $s1.

The loop will be executed four times. The values $s1 takes on will be 10, 9, 6, 5, 2, 1, -2, -3, -6. The final value will be -6.

6. (3 points) For the MAL instruction

```
          lw    $t1, 15($t2)
```

which statement is correct?

(a) The instruction will execute normally.

=> **(b)** The instruction will cause a trap.

(c) It is impossible to say whether (a) or (b) will occur.

7. (6 points) Suppose a procedure written in MAL uses registers $0, $s0, $s1, and $s3, and calls itself recursively. It receives four parameters, in registers $a0-$a3.

(a) Following MIPS RISC register usage conventions, what is the minimum size of the activation record required? Justify your answer.

Register $0 need not be saved. Registers $s0, $s1, and $s3 need to be saved. Register $ra needs to be saved. Space must be saved for the four parameters. Thus the total space needed is at least 8 words (32 bytes).

(b) If the procedure neither calls itself nor any other procedures, how much of the space required for your answer to part (a) can be eliminated? Justify your answer.

Must still preserve registers $s0, $s1, and $3 for calling procedure.

8. (4 points) The following hexadecimal numbers represent machine code. Give the corresponding TAL instruction.

(a) 0x90b30010

lbu $19, 16($5)

(b) 0x35050011

ori $5, $8, 0x11

9. (4 points) The Clock_Handler code from assignment 12 determines that a clock interrupt has occurred, and increments a counter. If the code did not check to see if a clock interrupt had occurred, but simply incremented the counter and cleared the clock status, what would the Clock_Handler be counting?

The total number of times an interrupt occurred.

10. (4 points) Consider the following code fragment and fill in the blank machine code.

Address	Machine code	TAL Instruction	
0x00400000	0xafbf0000	label: sw	$31, ($sp)
.		.	
.		.	
0x00400100	0x14a0ffb0	bne	$5, $0, label
.		.	
.		.	
0x00400200	0x0100000	j	label

11. (4 points) The following code fragment multiplies integers in register $s0 and $s1 together, storing the result in register $s2:

```
        .text
        mult   $s0, $s1
        mflo   $s2
        mfhi   $t0
        bgez   $s2, L1
        addu   $t0, $t0, 1
L1:     bnez   $t0, label
        ...
```

(a) What has happened if the code branches to `label`?

The multiplication resulted in overflow for 32-bit representation.

(b) Give an example *in decimal* of integer values in 2's complement that will cause the code to branch to `label`.

$s0: 1,000,000,000

$s1: 1,000,000,000

12. (6 points) Each of the following features is used in the I/O system of a computer in order to prevent certain difficulties that would otherwise arise. For each item below describe a problem that motivates its use. (Note: You are not asked to define what these items are, and you will not earn points for giving definitions.)

(a) Status words

The status word allows processing of an I/O request exactly once. An answer discussing the status register was also acceptable.

(b) Memory-mapped I/O

This permits I/O interactions without the need for additional instructions specifically for I/O.

(c) Traps

Traps make possible special treatment of instructions when an exceptional condition, such as overflow, occurs.

13. (3 points) Briefly give the circumstances under which no stack frame need be allocated for a procedure.

Procedures that require not storage for variables (temporaries or saved registers) and call no other procedures require no activation record.

14. (12 points) Synthesize the following MAL instructions with TAL instructions. If possible, use a single TAL instruction.

(a) `sub $8, $8, 5`

```
addi $8, $8, -5
```

(b) `li $8, -5`

```
addi $8, $0, -5
```

(c) `add $s0, $s0, 0x10000`

```
lui $1, 1
add $s0, $1, $s0
```

(d) `l.s $f4, ($t4)`

```
lwc1 $f4, ($t4)
```

(e) `putc 'X'`

```
addi $4, $0, 0x58
addi $2, $0, 11
syscall
```

(f) `mul $s1, $t1, $s1`

```
mult $t1, $s1
mflo $s1
```

15. (4 points) A MIPS RISC assembler allows the following addressing mode for a load instruction:

```
lw $21, label+8
```

An effective address is computed by adding the 32-bit address, given by `label`, to the constant 8. Give a TAL synthesis for this MAL instruction if `label` has been assigned the address 0x2468abcd.

```
lui   $1, 0x2468
ori   $1, 0xabcd
lw    $21, 8($1)
```